



1/5

Replacement Sheet

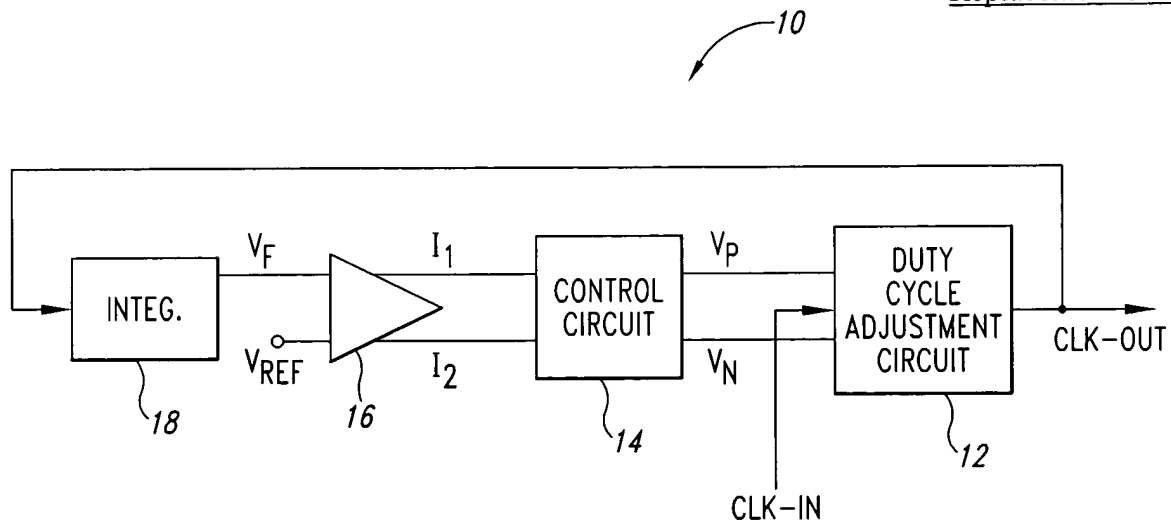


Fig. 1

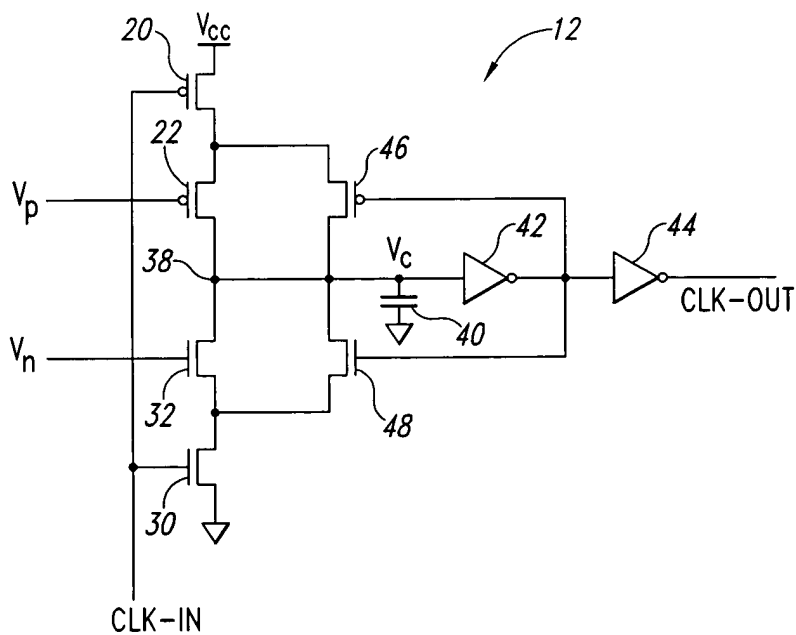


Fig. 2

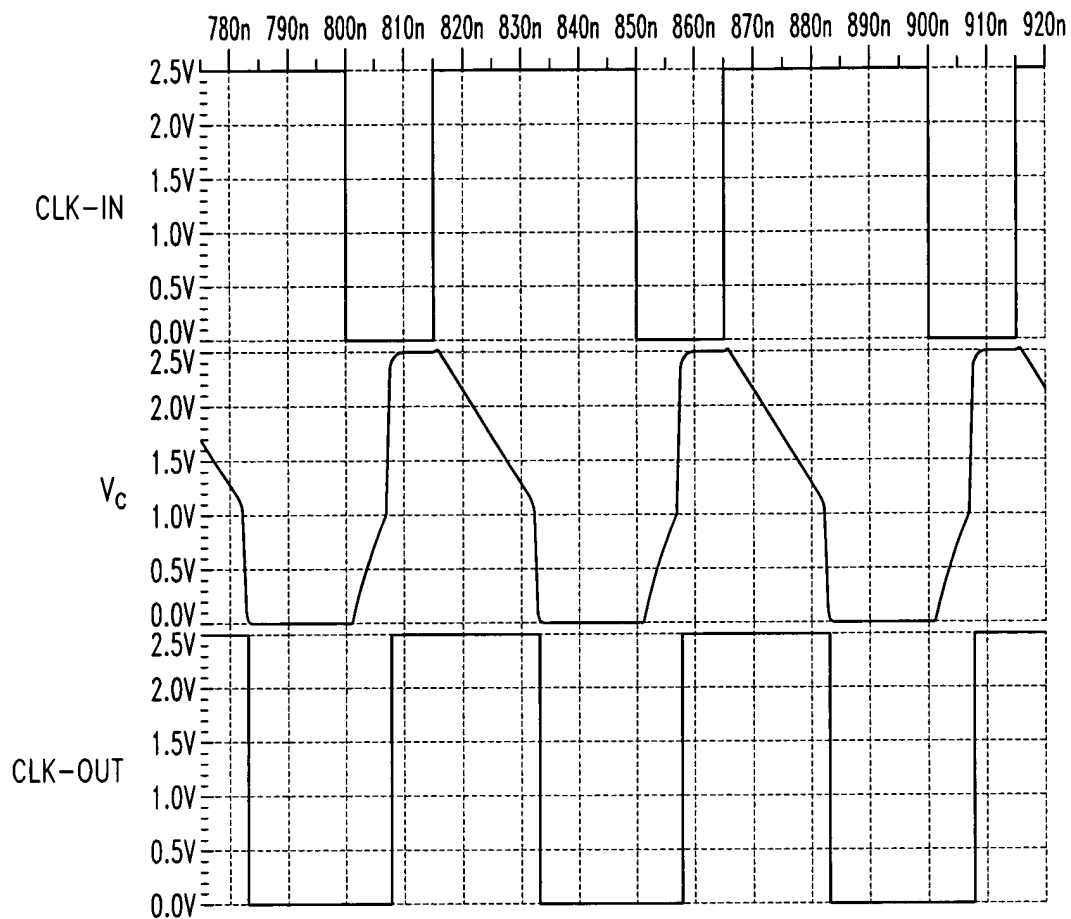


Fig. 3

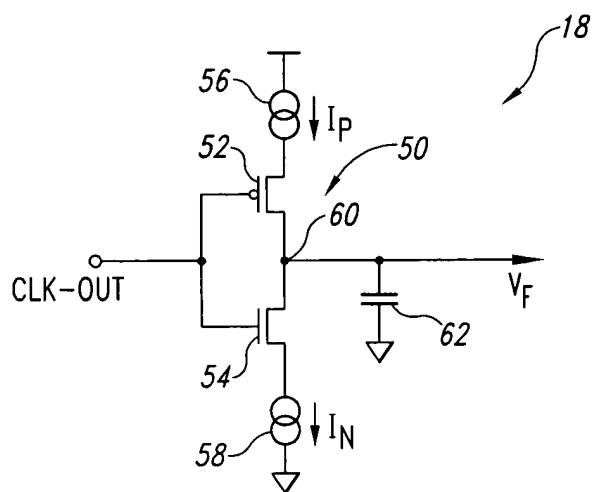
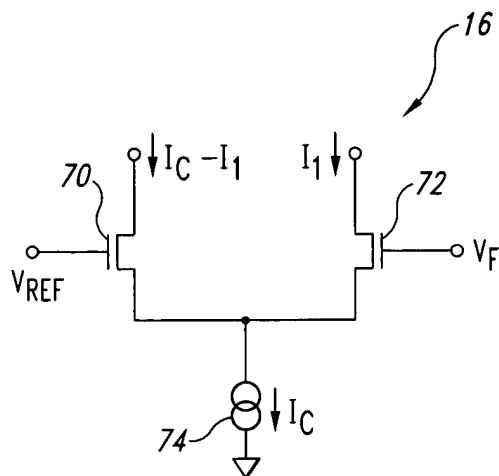
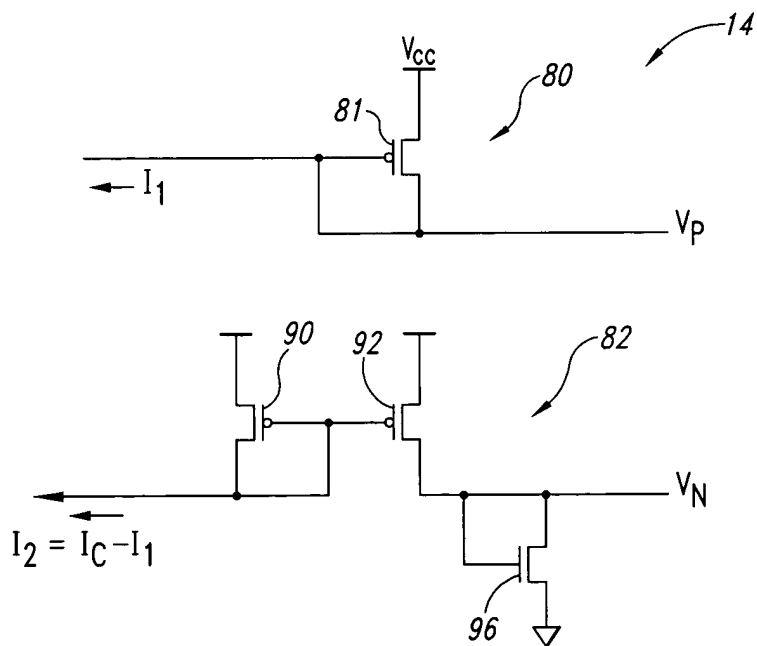


Fig. 4

*Fig. 5**Fig. 6*

Block diagram of a memory system 110. The system includes a MEMORY ARRAY 120, a CONTROL LOGIC CIRCUIT 114, an ADDRESS DECODER 116, and a READ/WRITE CIRCUIT 118. External signals CLK, CKE, CONTROL BUS, ADDRESS BUS, and DATA BUS enter from the left. CLK-ADT is an internal signal. The CONTROL LOGIC CIRCUIT 114 is connected to CLK-ADT, CLK, CKE, and the CONTROL BUS. The ADDRESS DECODER 116 is connected to the CONTROL LOGIC CIRCUIT 114, the ADDRESS BUS, and the MEMORY ARRAY 120. The READ/WRITE CIRCUIT 118 is connected to the ADDRESS DECODER 116, the DATA BUS, and the MEMORY ARRAY 120. A block 18 is connected to CLK and CLK-ADT.

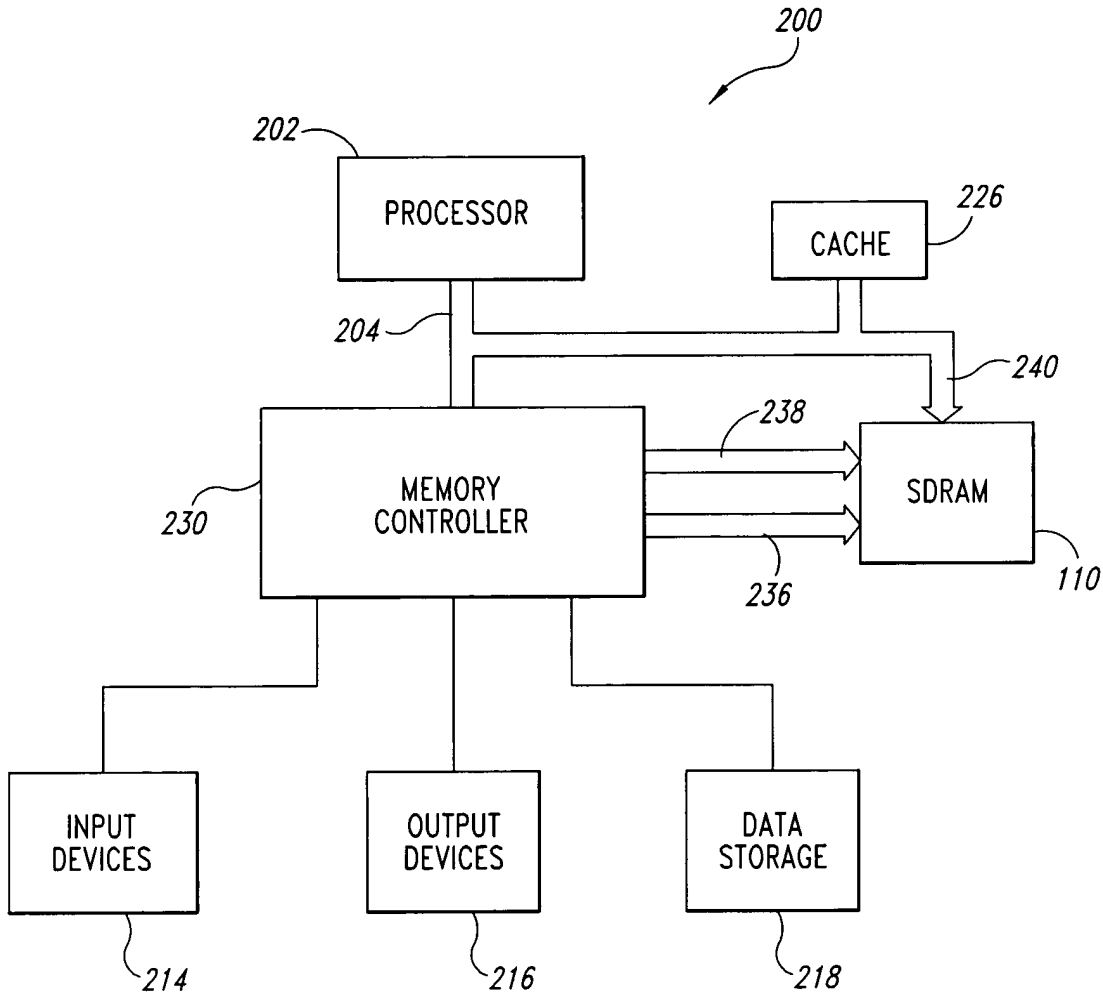


Fig. 8